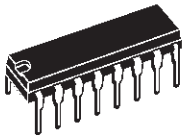
# M74HCT7259

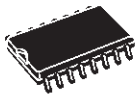
## 8BIT ADDRESSABLE LATCH/DECODER/RELAIS DRIVER (OPEN DRAIN,INVERTING OUTPUT)

**PRELIMINARY DATA**

- LOW POWER DISSIPATION
  $I_{CC}$ = 4 µA (MAX.) AT $T_A$ = 25 °C
- COMPATIBLE WITH TTL OUTPUTS
  $V_{IH}$ = 2V (MIN) $V_{IL}$ = 0.8V (MAX) AT 5V
- OUTPUT DRIVE CAPABILITY
  90 LSTTL LOADS
- HIGH CURRENT OPEN DRAIN OUTPUT UP TO 80 mA



**DIP**



**SOP**

| ORDER CODES | | |
|---|---|---|
| **PACKAGE** | **TUBE** | **T & R** |
| DIP | M74HCT7259B1R | |
| SOP | M74HCT7259M1R | M74HCT7259M1RTR |

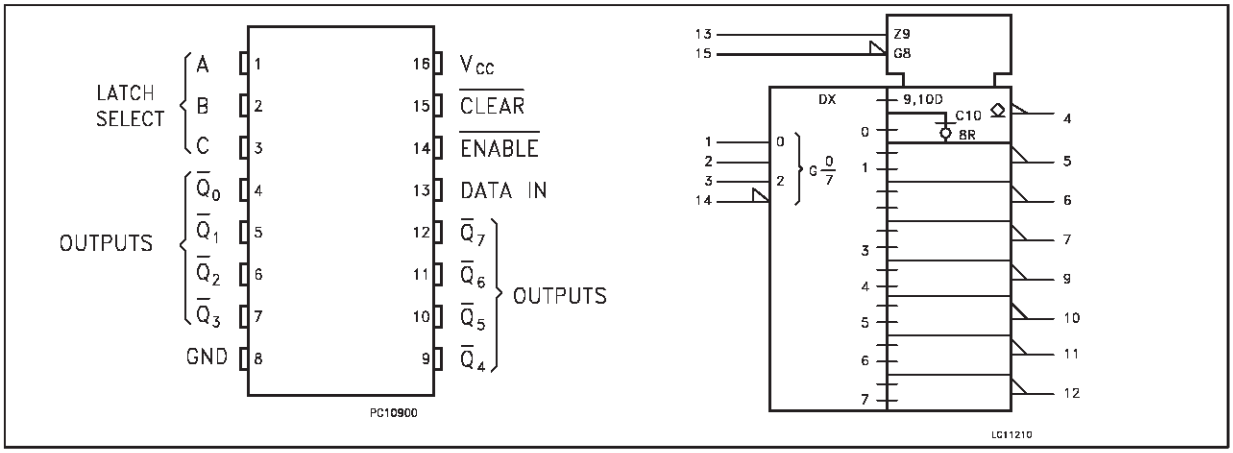
The M74HCT7259 is a high speed CMOS 8 BIT ADDRESSABLE LATCH/DECODER fabricated in silicon gate C2MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption.

The M74HCT7259 has single data input (D) 8 LATCH inverted OUTPUTS ($\overline{Q0}$-$\overline{Q7}$), 3 address inputs (A, B and C), common enable input ($\overline{ENABLE}$) and a common $\overline{CLEAR}$ input. To operate this device as an addressable latch, data is held on the D input, and the address of the latch into which the data is to be entered is held on the A, B and C inputs.

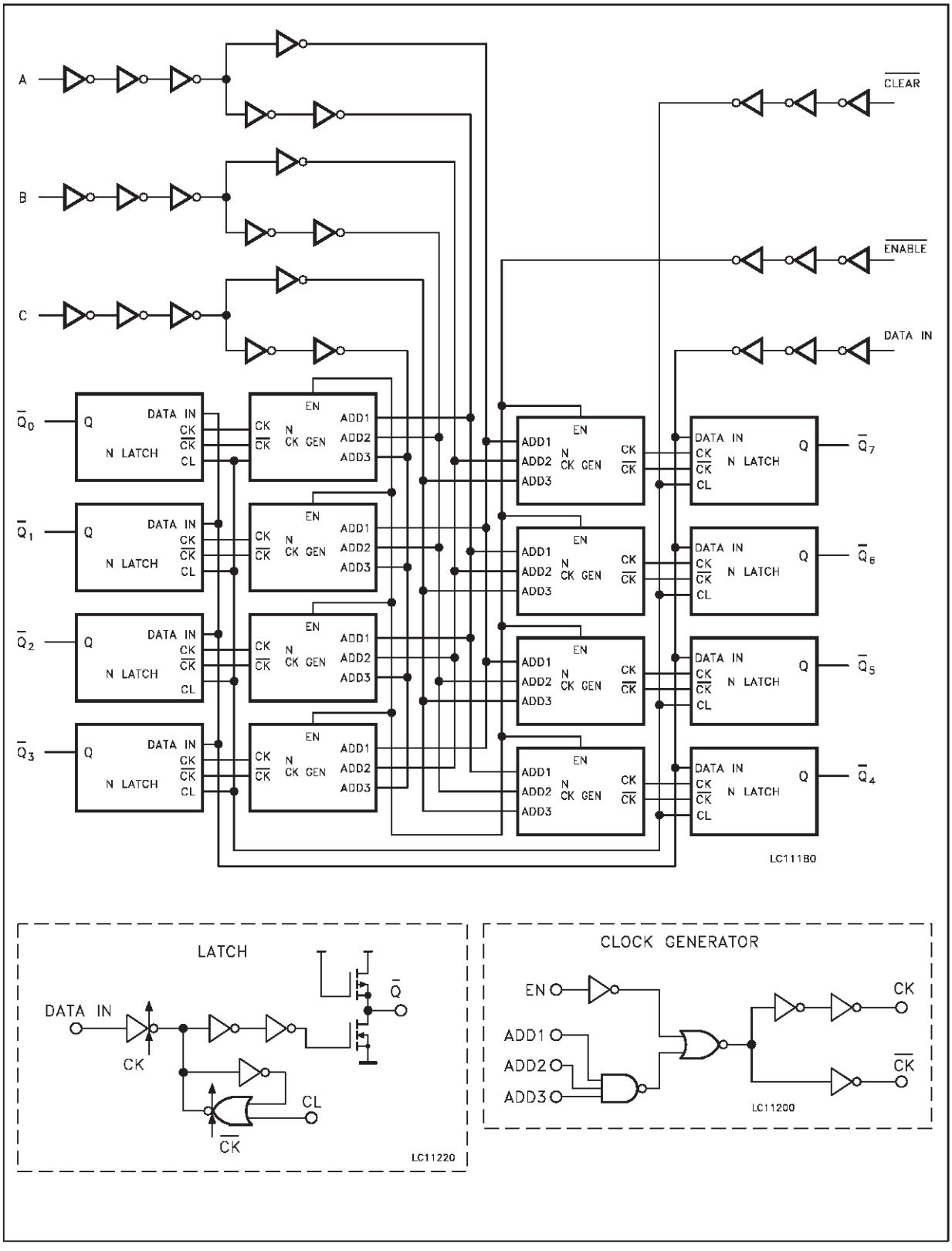
When $\overline{ENABLE}$ is taken low the data flows through to the address output. The data is stored on the positive-going edge of the $\overline{ENABLE}$ pulse. All unadressed latches will remain unaffected. With $\overline{ENABLE}$ in the high state the device is deselected and all latches remain in their previous state, unaffected by changes on the data or address inputs. To eliminate the possibility of entering erroneous data into the latches, the $\overline{ENABLE}$ should be held high (inactive) while the address lines are changing. If $\overline{ENABLE}$ is held high and $\overline{CLEAR}$ is taken low all eight latches are cleared to the HIGH (OFF) state. If $\overline{ENABLE}$ is low all latches except the addressed latch will be cleared. The address latch will instead be the complement of the D input,effectively implementing a 3 to 8 line decoder. Internal clamp diodes protect the open drain outputs against over voltages due to inductive loads.

All inputs are equipped with protection circuits against static discharge and transient excess voltage.

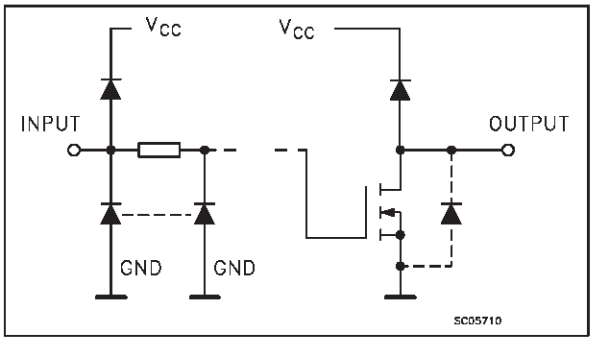
### PIN CONNECTION AND IEC LOGIC SYMBOLS



## LOGIC DIAGRAM



## INPUT EQUIVALENT CIRCUIT




## PIN DESCRIPTION

| PIN No | SYMBOL | NAME AND FUNCTION |
|---|---|---|
| 1, 2, 3 | A, B, C | Latch Select |
| 4, 5, 6, 7, 9, 10, 11, 12 | $\overline{Q0}$ to $\overline{Q7}$ | latch Outputs |
| 13 | DATA IN | Data Inputs |
| 14 | $\overline{ENABLE}$ | Latch Enable Input |
| 15 | $\overline{CLEAR}$ | Conditional Reset Input |
| 8 | GND | Ground (0V) |
| 16 | $V_{CC}$ | Positive Supply Voltage |

## TRUTH TABLE

| INPUTS | | OUTPUTS OF ADDRESSED LATCH | EACH OTHER OUTPUT | FUNCTION |
|---|---|---|---|---|
| $\overline{CLEAR}$ | $\overline{ENABLE}$ | | | |
| H | L | $\overline{D}$ | QI0 | ADDRESSABLE LATCH |
| H | H | Qi0 | Qi0 | MEMORY |
| L | L | $\overline{D}$ | H | 8-LINE DEMULTIPLEXER |

| SELECT INPUTS | | | LATCH ADDRESSED |
|---|---|---|---|
| C | B | A | |
| L | L | L | $\overline{Q0}$ |
| L | L | H | $\overline{Q1}$ |
| L | H | L | $\overline{Q2}$ |
| L | H | H | $\overline{Q3}$ |
| H | L | L | $\overline{Q4}$ |
| H | L | H | $\overline{Q5}$ |
| H | H | L | $\overline{Q6}$ |
| H | H | H | $\overline{Q7}$ |

D: The level at the data input
Qi0: The level before the indicated steady state input conditions were established, (i = 0,1,....,7).

## ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{CC}$ | Supply Voltage | -0.5 to +7.0 | V |
| $V_I$ | DC Input Voltage | -0.5 to $V_{CC}$ + 0.5 | V |
| $V_O$ | DC Output Voltage | -0.5 to $V_{CC}$ + 0.5 | V |
| $I_{IK}$ | DC Input Diode Current | ± 20 | mA |
| $I_{OK}$ | DC Output Diode Current | ± 20 | mA |
| $I_O$ | DC Output Current Per Pin | 100 | mA |
| $I_{GND}$ | Ground Current | - 800 | mA |
| $I_{CC}$ | DC $V_{CC}$ Current | 50 | mA |
| $P_D$ | Power Dissipation | 500 (*) | mW |
| $T_{stg}$ | Storage Temperature | -65 to +150 | °C |
| $T_L$ | Lead Temperature (10 sec) | 300 | °C |

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.
(*) 500 mW: ≅ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{CC}$ | Supply Voltage | 3.3 to 5.5 | V |
| $V_I$ | Input Voltage | 0 to $V_{CC}$ | V |
| $V_O$ | Output Voltage | 0 to $V_{CC}$ | V |
| $T_{op}$ | Operating Temperature | -40 to +85 | $^oC$ |
| dt/dv | Input Rise and Fall Time | 0 to 500 | ns |

## DC SPECIFICATIONS

| Symbol | Parameter | Test Conditions | | Value | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | $V_{CC}$ (V) | | $T_A$ = 25 $^oC$ | | | -40 to 85 $^oC$ | | |
| | | | | Min. | Typ. | Max. | Min. | Max. | |
| $V_{IH}$ | High Level Input Voltage | 3.3(*) | | 2.0 | | | 2.0 | | V |
| | | 4.5 to 5.5 | | 2.0 | | | 2.0 | | |
| $V_{IL}$ | Low Level Input Voltage | 3.3(*) | | | | 0.5 | | 0.5 | V |
| | | 4.5 to 5.5 | | | | 0.8 | | 0.8 | |
| $V_{OL}$ | Low Level Output Voltage | 3.3(*) | $I_O$= 70 mA | | 0.4 | 0.5 | | 0.6 | V |
| | | 4.5 | $I_O$= 20 µA | | 0.0 | 0.1 | | 0.1 | |
| | | | $I_O$= 36 mA | | 0.17 | 0.26 | | 0.33 | |
| | | | $I_O$= 80 mA | | 0.32 | 0.40 | | 0.50 | |
| $I_{OZ}$ | Output Leackage Current | 5.5 | $V_I$ = $V_{IH}$ or $V_{IL}$<br>$V_{OUT}$ = $V_{CC}$ or GND | | | ±5 | | ±50 | µA |
| $I_{IN}$ | Input Leakage Current | 5.5 | $V_I$ = $V_{CC}$ or GND | | | ±0.1 | | ±1 | µA |
| $I_{CC}$ | Quiescent Supply Current | 5.5 | $V_I$ = $V_{CC}$ or GND | | | 4 | | 40 | µA |
| | | | Each Input in Turn:<br>$V_{IN}$ = 0.5 V or 2.4 V<br>All Other Inputs:<br>$V_{CC}$ or GND | | | 3.0 | | 3.9 | mA |

(*) Voltage Range is 3.3V ±5%

**AC ELECTRICAL CHARACTERISTICS** ($C_L$ = 50 pF, Input $t_r = t_f$ = 6 ns)

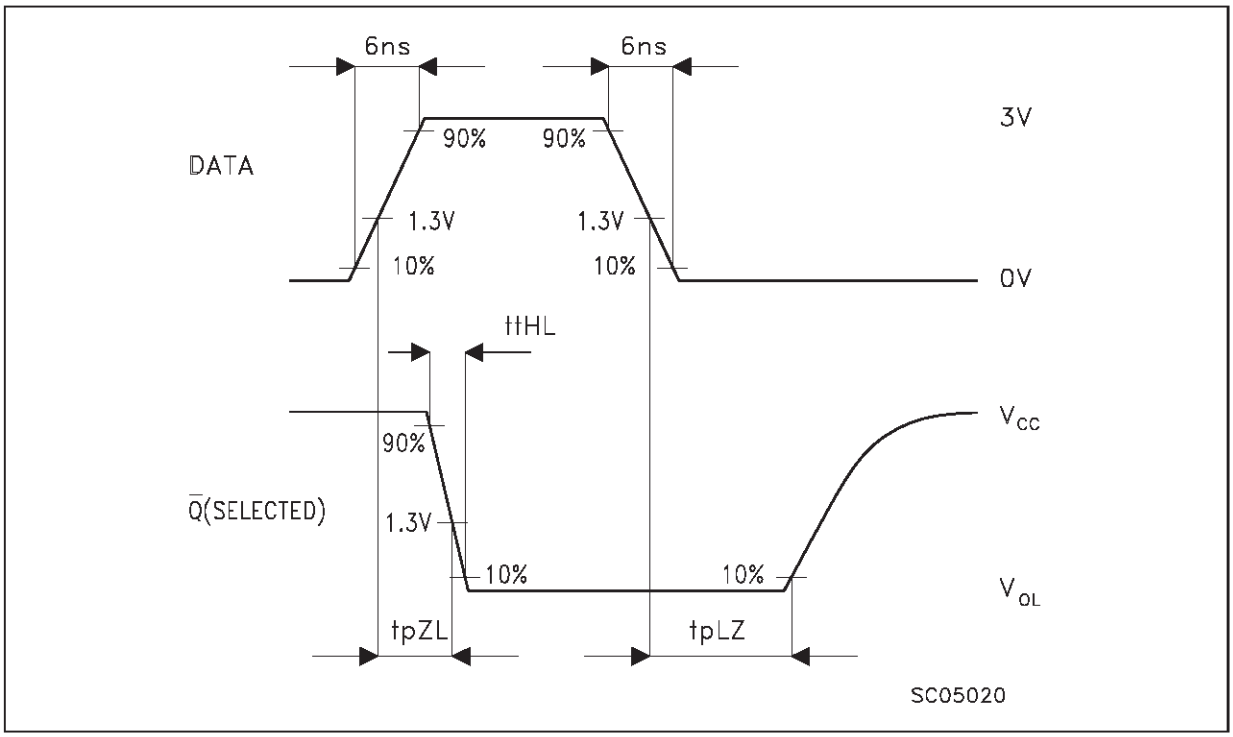
| Symbol | Parameter | Test Conditions | | | Value | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | $V_{CC}$ (V) | $C_L$ (pF) | $R_L$ (KΩ) | $T_A$ = 25 °C | | | -40 to 85 °C | | |
| | | | | | Min. | Typ. | Max. | Min. | Max. | |
| $t_{TLH}$ | Output Transition Time | 3.3(*) | 50 | 1 | | | | | 18 | ns |
| | | 4.5 | 50 | 1 | | 3 | 6 | | 9 | |
| $t_{PLZ}$ $t_{PZL}$ | Propagation Delay Time (DATA - $\overline{Q}$) | 3.3(*) | 50 | 1 | | | | | 80 | ns |
| | | 3.3(*) | 150 | 1 | | | | | 92 | |
| | | 4.5 | 50 | 1 | | 20 | 31 | | 39 | |
| | | 4.5 | 150 | 1 | | 24 | 37 | | 46 | |
| $t_{PLZ}$ $t_{PZL}$ | Propagation Delay Time (A, B, C - $\overline{Q}$) | 3.3(*) | 50 | 1 | | | | | 98 | ns |
| | | 3.3(*) | 150 | 1 | | | | | 112 | |
| | | 4.5 | 50 | 1 | | 25 | 39 | | 49 | |
| | | 4.5 | 150 | 1 | | 29 | 45 | | 56 | |
| $t_{PLZ}$ $t_{PZL}$ | Propagation Delay Time ($\overline{ENABLE}$ - $\overline{Q}$) | 3.3(*) | 50 | 1 | | | | | 82 | ns |
| | | 3.3(*) | 150 | 1 | | | | | 98 | |
| | | 4.5 | 50 | 1 | | 21 | 33 | | 41 | |
| | | 4.5 | 150 | 1 | | 25 | 39 | | 49 | |
| $t_{PLZ}$ $t_{PZL}$ | Propagation Delay Time ($\overline{CLEAR}$ - $\overline{Q}$) | 3.3(*) | 50 | 1 | | | | | 76 | ns |
| | | 3.3(*) | 150 | 1 | | | | | 90 | |
| | | 4.5 | 50 | 1 | | 19 | 30 | | 38 | |
| | | 4.5 | 150 | 1 | | 23 | 36 | | 45 | |
| $t_{W(L)}$ | Minimum Pulse Width ($\overline{CLEAR}$) | 3.3(*) | 50 | 1 | | | | | 38 | ns |
| | | 4.5 | 50 | 1 | | 7 | 15 | | 19 | |
| $t_{W(L)}$ | Minimum Pulse Width ($\overline{ENABLE}$) | 3.3(*) | 50 | 1 | | | | | 38 | ns |
| | | 4.5 | 50 | 1 | | 7 | 15 | | 19 | |
| $t_s$ | Minimum Set-Up Time | 3.3(*) | 50 | 1 | | | | | 26 | ns |
| | | 4.5 | 50 | 1 | | 4 | 10 | | 13 | |
| $t_h$ | Minimum Hold Time | 3.3(*) | 50 | 1 | | | | | 10 | ns |
| | | 4.5 | 50 | 1 | | | 5 | | 5 | |
| $C_{IN}$ | Input Capacitance | | | | | 5 | 10 | | 10 | pF |
| $C_{PD}$ (**) | Power Dissipation Capacitance | | | | | 96 | | | | pF |

(*) Voltage Range is 3.3V ±5%

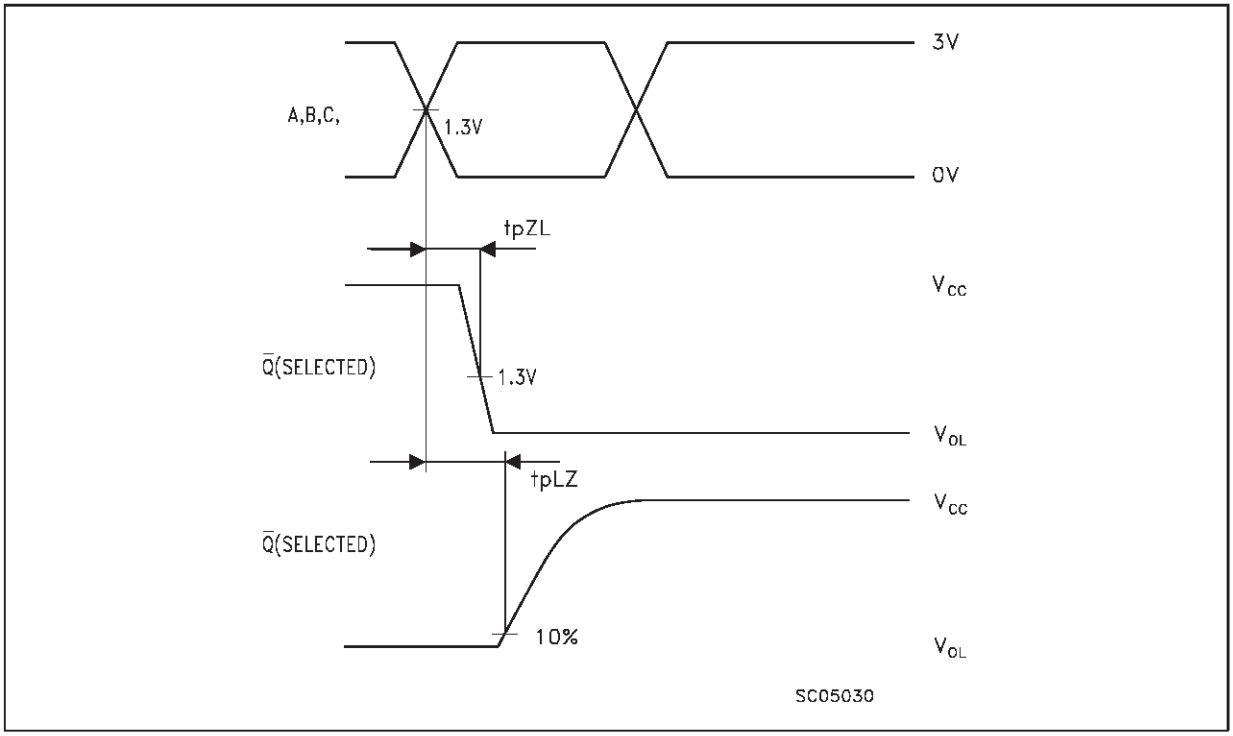
(**) $C_{PD}$ is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operting current can be obtained by the following equation. $I_{CC}(opr) = C_{PD} \bullet V_{CC} \bullet f_{IN} + I_{CC}$

## SWITCHING CHARACTERISTICS TEST WAVEFORMS

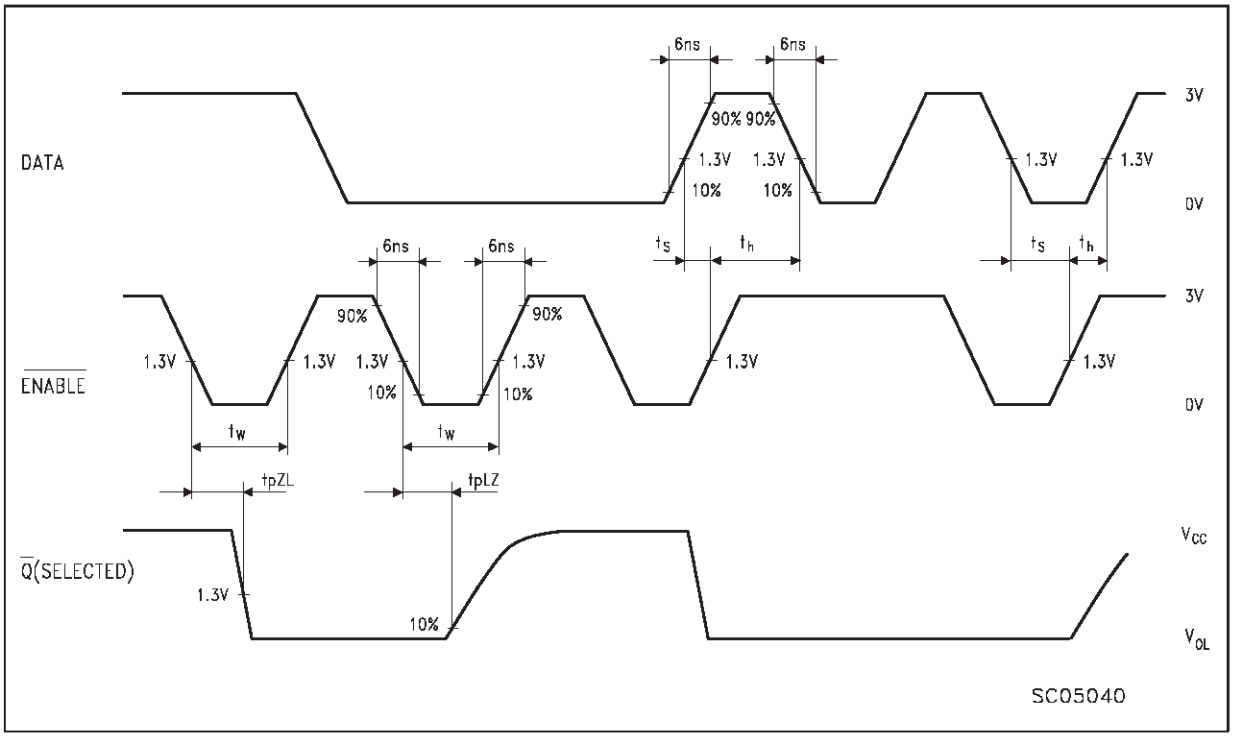
WAVEFORM 1: ($\overline{\text{ENABLE}}$ = L, $\overline{\text{CLR}}$ = H, A-C= STABLE)



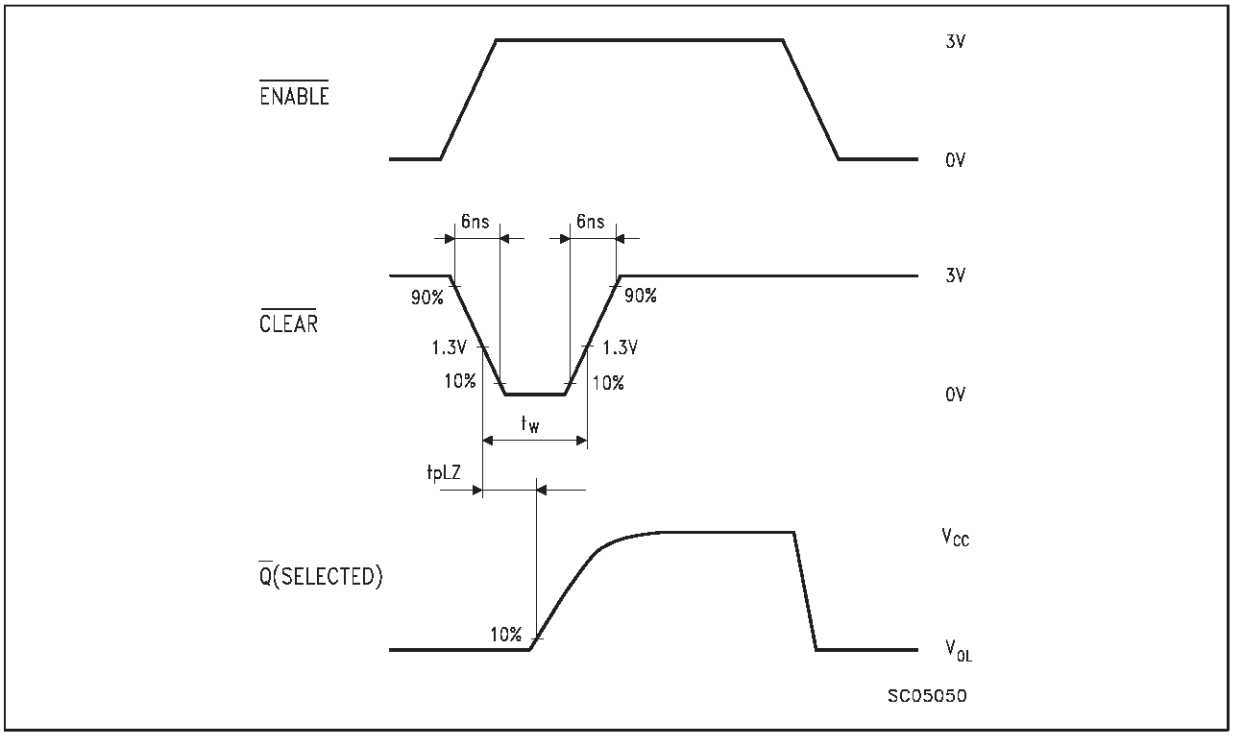

WAVEFORM 2: ($\overline{\text{ENABLE}}$ = L)



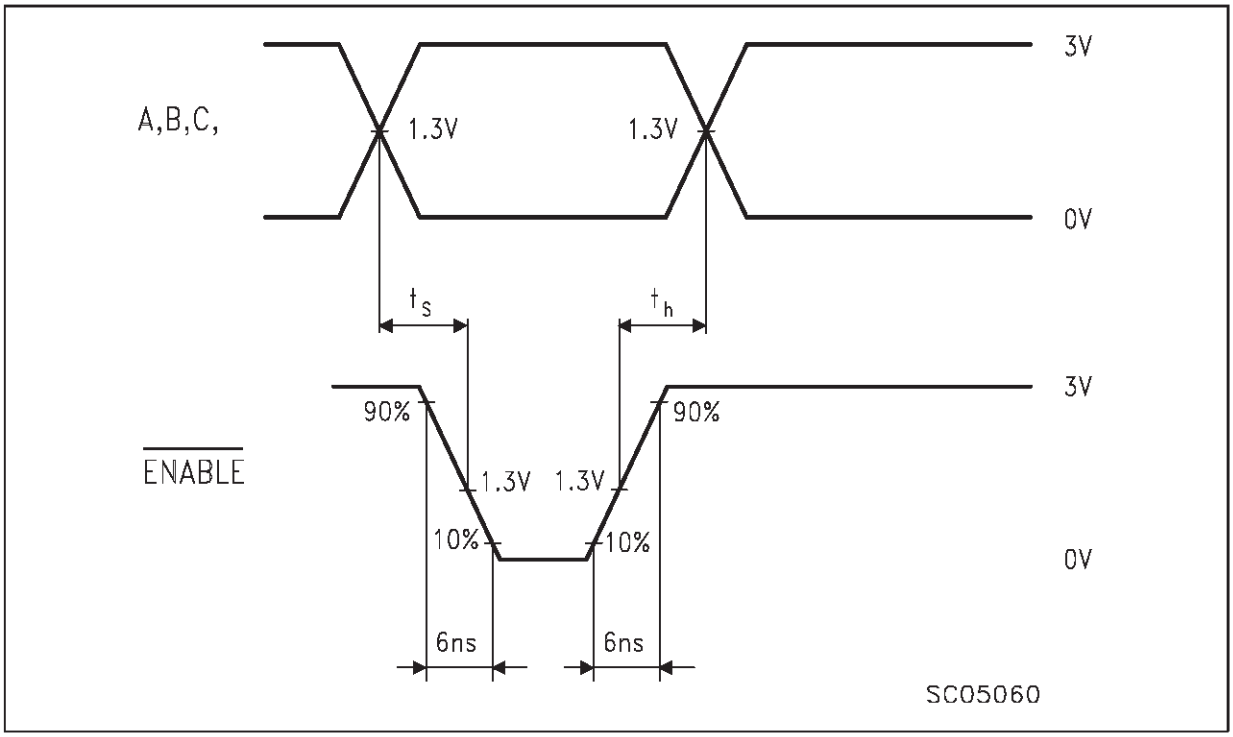
WAVEFORM 3: ($\overline{CLR}$ = H, A-C = STABLE)



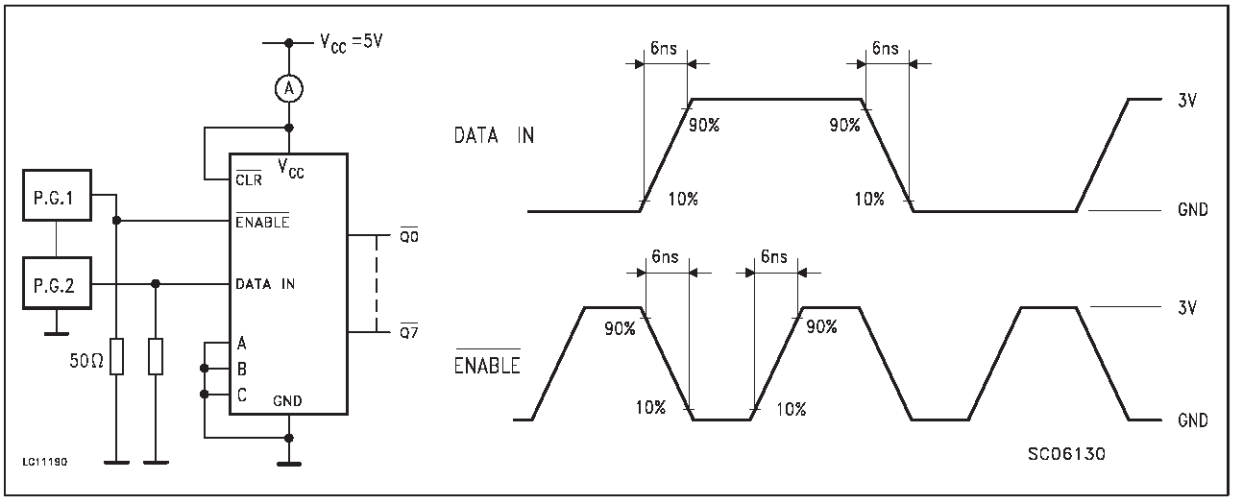

WAVEFORM 4: (D = H, A-C = STABLE)



WAVEFORM 5: ($\overline{CLR}$ = H)

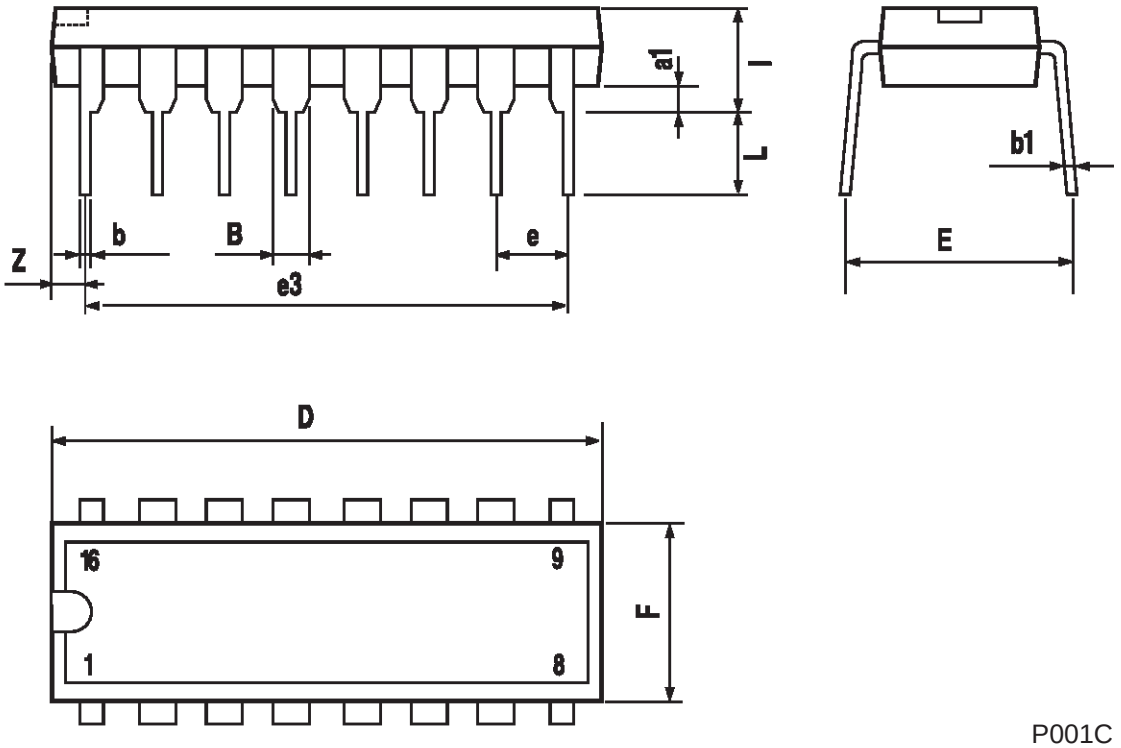



TEST CIRCUIT $I_{CC}$ (Opr.)



## Plastic DIP-16 (0.25) MECHANICAL DATA

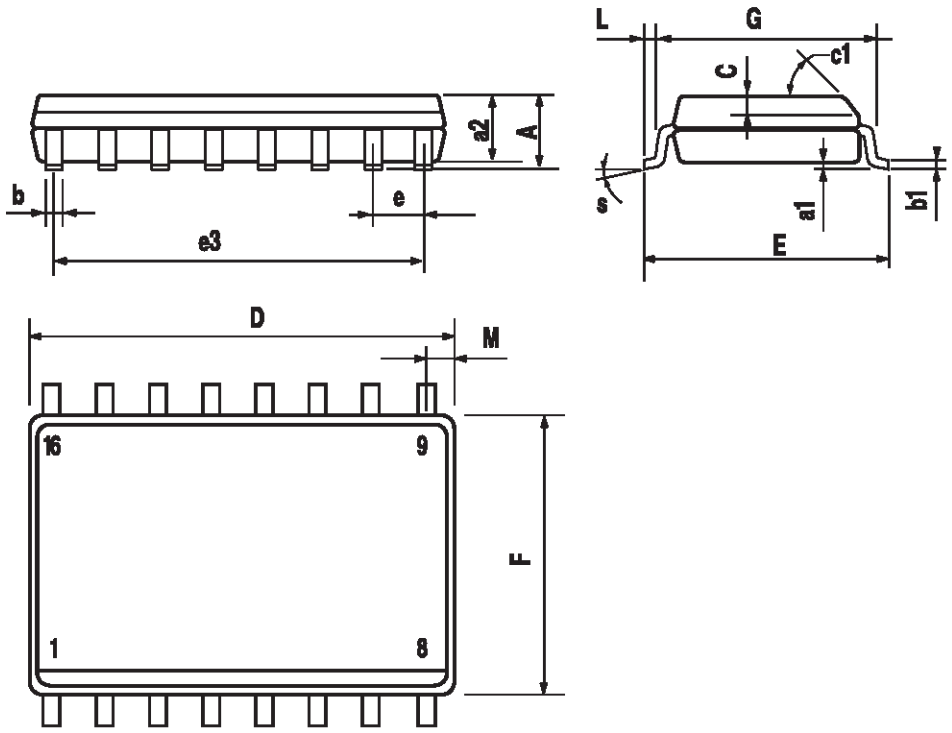
| DIM. | mm | | | inch | | |
|---|---|---|---|---|---|---|
| | MIN. | TYP. | MAX. | MIN. | TYP. | MAX. |
| a1 | 0.51 | | | 0.020 | | |
| B | 0.77 | | 1.65 | 0.030 | | 0.065 |
| b | | 0.5 | | | 0.020 | |
| b1 | | 0.25 | | | 0.010 | |
| D | | | 20 | | | 0.787 |
| E | | 8.5 | | | 0.335 | |
| e | | 2.54 | | | 0.100 | |
| e3 | | 17.78 | | | 0.700 | |
| F | | | 7.1 | | | 0.280 |
| I | | | 5.1 | | | 0.201 |
| L | | 3.3 | | | 0.130 | |
| Z | | | 1.27 | | | 0.050 |




P001C

## SO16L MECHANICAL DATA

| DIM. | mm | | | inch | | |
|---|---|---|---|---|---|---|
| | MIN. | TYP. | MAX. | MIN. | TYP. | MAX. |
| A | | | 2.65 | | | 0.104 |
| a1 | 0.1 | | 0.2 | 0.004 | | 0.008 |
| a2 | | | 2.45 | | | 0.096 |
| b | 0.35 | | 0.49 | 0.014 | | 0.019 |
| b1 | 0.23 | | 0.32 | 0.009 | | 0.012 |
| C | | 0.5 | | | 0.020 | |
| c1 | 45 (typ.) | | | | | |
| D | 10.1 | | 10.5 | 0.397 | | 0.413 |
| E | 10.0 | | 10.65 | 0.3.93 | | 0.419 |
| e | | 1.27 | | | 0.050 | |
| e3 | | 8.89 | | | 0.350 | |
| F | 7.4 | | 7.6 | 0.291 | | 0.300 |
| L | 0.5 | | 1.27 | 0.020 | | 0.050 |
| M | | | 0.75 | | | 0.029 |
| S | 8 (max.) | | | | | |




P013I